# Design and Basic Blocks of a Neuromorphic VLSI Analogue Vision System

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***Abstract:*** *In this paper we present a complete neuromorphic image processing system and we report the development of an integrated CMOS low-power circuit to test the feasibility of its different stages. The image system consists of different parallel-processing stages: phototransduction, non-linear filtering, oscillatory segmentation network and post-processing to extract fundamental characteristics. The circuit presented emulates parts of the behaviour of biological neural networks as found in the retina and the visual cortex of living beings, adopting the neuromorphic approach that takes advantage of analogue VLSI electronics. The final objective is to develop a small and low-power system embedded in a single focal-plane integrated circuit to be used in portable applications. Each stage is briefly described. Simulations and experimental results of some basic blocks are also reported.*

## 1. Introduction

The commonly used digital approach to solving electronic problems has some important advantages as flexibility, precision and moderate design complexity compared to other alternatives as analogue ones. However, the latter have some advantages that should be considered for small and low-power electronic systems which are required for the increasing market of portable applications. The main advantage is the possibility of reducing power consumption and area overhead, which are improved when used in large scale of integration technologies.

On the other hand, living beings seem to have already solved the problem of building successful tiny and energy-efficient systems. A simple fly is more capable of finding food and escaping from danger in a smallest and less power eager system than the most complex artificial computer that can be built.

Taking advantage of both worlds, the increasing microelectronics developments and the better knowledge of the nervous system of animals, in the late eighties, C. Mead [1] proposed a new approach to solving the problem of small and low-power systems. The so-called neuromorphic approach consists in emulating the complex neural system of living beings using the latest VLSI technology.

The neuromorphic approach has been widely applied to vision problems, especially to first stages or low-level vision. These processes are commonly performed at the retina of living beings and consist in spatially and temporally filtering images, reducing noise or extracting basic visual characteristics. Several

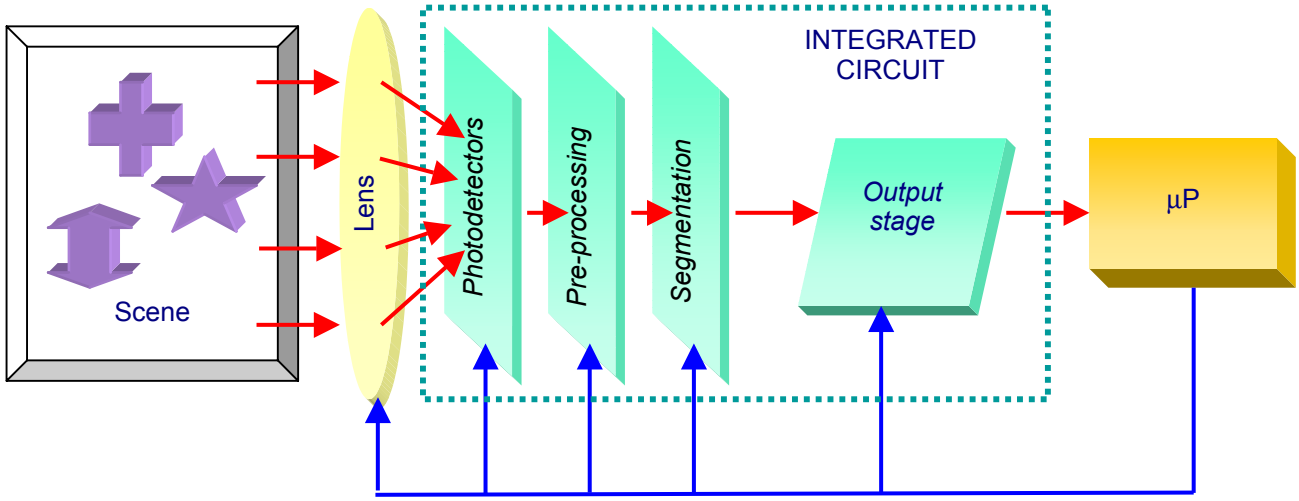



**Figure 1:** VLSI neuromorphic Image Segmentation System

realizations at this low-level stage are reported in the literature [2] [3]. However, higher level processing stages that take place in the visual cortex as attention or segmentation of images have not drawn such attention under the neuromorphic perspective [4] [5] [6].

The oscillatory nature of visual cortex neurons has been largely studied by biologists and computer scientists [7] [8] and synchronization phenomena has been observed. This studies have been used to create models of brain-like computing systems [9] [10] that can segment real images successfully when simulated on computers.

Few implementations of electronic oscillatory systems exist [5] [6] and they mainly consist in the segmentation stage. In this paper we propose a complete system consisting of different stages using analogue electronics to reduce power consumption and overhead area bearing in mind autonomous electronic applications. The system we propose consists of different stages that are located in the retina and the visual cortex of living beings:

1.- Light sensing
2.- Pre-processing using non-linear filters
3.- Segmentation using an oscillatory network
4.- Post processing and results extraction

All these stages are fully parallel and the only output is the result after information is fully processed, thus there is no need of large communication bandwidth with associated bottlenecks to output large quantities of information as bitmap images.

**2. System architecture**

In Figure 1, the global system architecture is shown. The input image is projected onto a photodetector array by means of a lens. Transduced light is then pre-processed by two stages that first filter noise and small luminance differences and after enhance neighbour pixels with equal or similar luminance. The pre-processing stage output determines neighbour coupling degree of a coupled-oscillator array that performs the segmentation stage. At this stage scene objects are segregated by means of phase-encoding. The output stage generates several informations about the image besides of the detected segments. In particular the associated centroids and size and number of objects are obtained. An external microprocessor reads network results and controls each stage parameters for an appropriate segmentation and/or scene attention guidance.

All the processing stages, except microprocessor, perform in focal-plane. Since models use mostly local computation, interconnect distribution is not a big issue as could be in other models.

In Figure 2, a simplified, three-element view of the integrated circuit is represented. For the sake of simplicity, only three pixels in a one-dimension configuration are depicted, but extension to more pixels in two dimensions is straightforward. An array of photodiodes (1) performs a light transducer stage. A logarithmic amplifier stage (2) extends the system dynamic range. Non-linear spatial filtering is done by means of a resistance and a resistive fuse mesh (3). Then data are applied to peak-shaped functions (4) that detect similarity of neighbours. An array of coupled oscillators (5) together with a Global Oscillator (GO) inhibitory cell (6) perform a modified LEGION [10] algorithm that was adapted for a simple VLSI implementation [5]. Finally, a resistance mesh (7) allows object centroid computation.

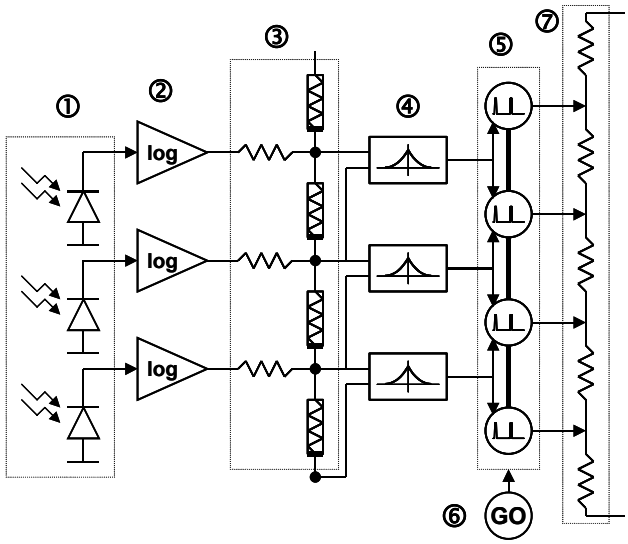



**Figure 2:** Simplified structure of a 1D, three-element, integrated circuit.

**3. Preprocessing stage**

After light transducing and logarithmic amplifying, non-linear spatial filtering is performed. The filter employs resistive fuse circuits [11] that perform spatial smoothing of noise and low-contrast features while preventing object boundaries to blur. Figure 3 displays the current-voltage (I-V) characteristic of the fuse and the PMOS-transistor version of a circuit that implements it [11], since a CMOS n-well technology is used. Below a given $V_{off}$ threshold between adjacent pixels luminance, the device behaves as a resistor, but above $V_{off}$ it changes its behaviour and remains open (flowing current becomes null). This is achieved by the circuit as follows. Transistor M7 operates as a resistor connected to input voltages Va and Vb. These voltages are also compared by a differential amplifier structure, formed by M1, M2, M3, M10 and M11. Each output branch of the amplifier controls transistors M8 and M9, that switch off the M7 resistor connection between Va and Vb when the differential input voltage is not small

enough. To become independent to the brightness level, the circuit also has common-mode compensation (formed by M4-M6) that keeps a similar resistance characteristic for a given differential input voltage regardless to its common level.

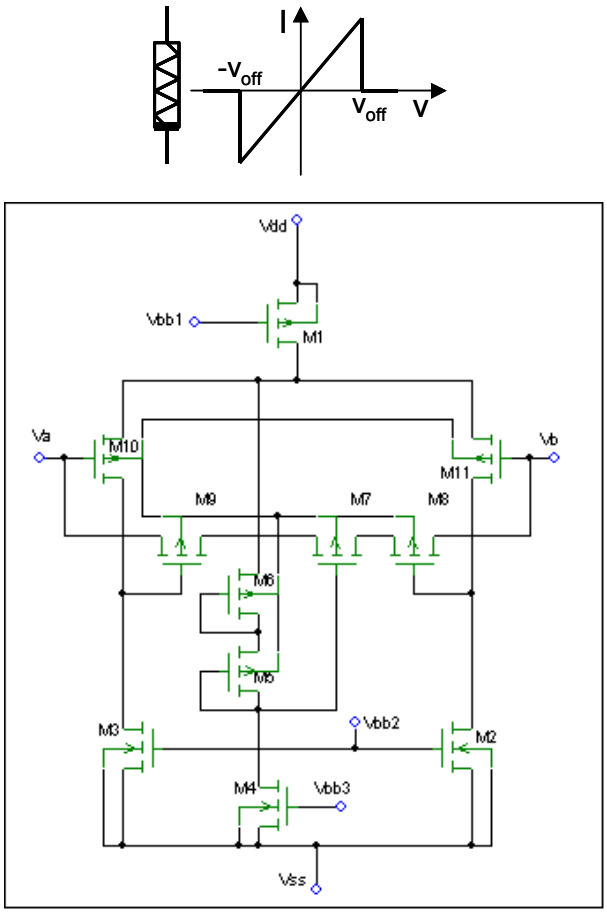



**Figure 3:** I-V characteristic of the resistive fuse and a PMOS circuit implementation.

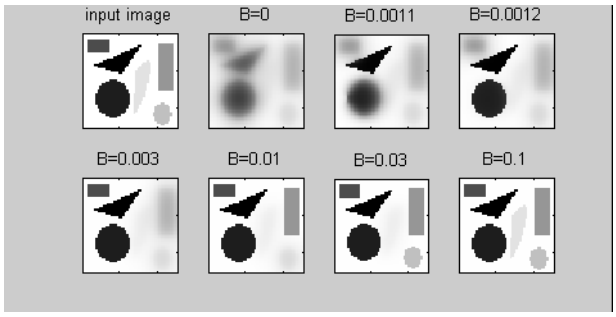
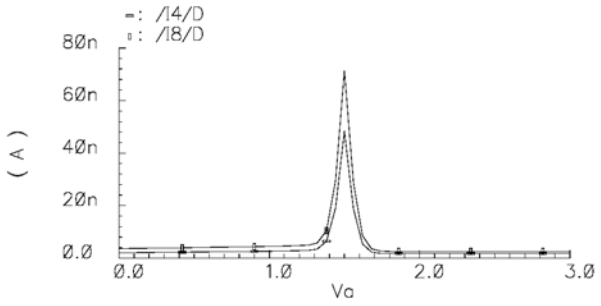



**Figure 4:** Simulations of the non-linear filter applied to an artificial image.

Figure 4 shows global simulation results of applying resistive fuse filtering to an artificial image containing objects with different levels of contrast. By changing parameter B, which is inversely proportional to $V_{off}$ parameter, several degrees of filtering can be obtained. Also, simulations have been reported for simple real images [12].

In addition to resistive fuse filtering, a local-response function is required since excitation of synapses that connect neighbour oscillators has to become maximum when brightness of the associated adjacent pixels is the same. Local functions reported in the literature such as Delbrück's bump function [13] could be used; however flat form of the function around the maximum value does not provide a good discrimination of similar pixels, so a peak-shaped function is more appropriate for our application. Therefore, a specific cell whose circuit implementation is shown in Figure 5 was developed. Simulation shows the desired peak shape.



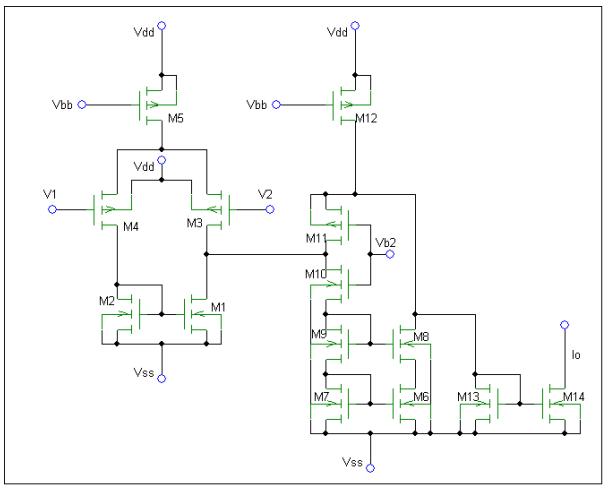




**Figure 5:** Peak-shaped circuit.

First stage (left hand side) is a differential amplifier that transduces input voltage into current. Output current of first stage is either positive or negative depending on the differential input voltage sign and zero when input voltages are equal ($V_1$=$V_2$). The second stage is simply a current rectifier and current-level shifter. This way, the circuit output current is maximum

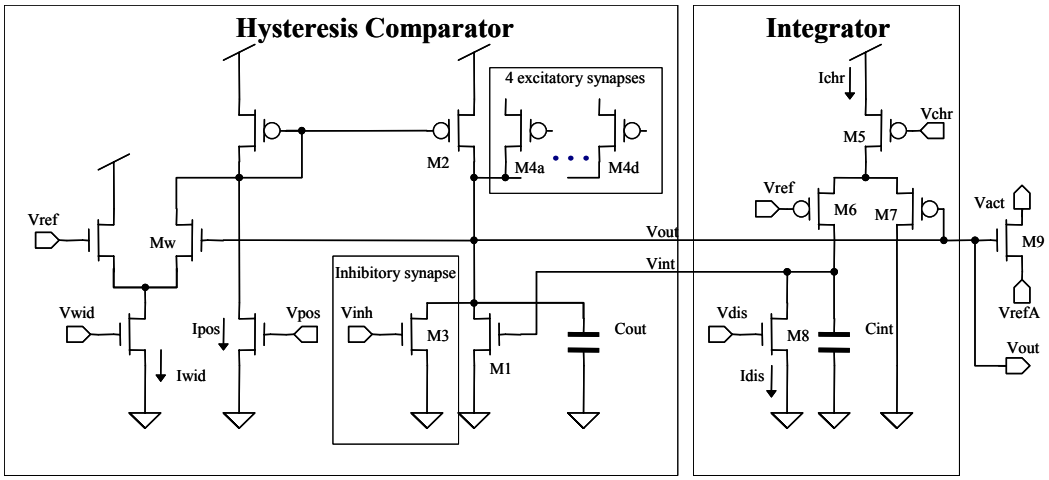



**Figure 7:** Schematic of the basic oscillator of the segmentation stage

when $V_1=V_2$ and it decreases with a peak shape as the input differential voltage absolute value increases.

**4. Segmentation stage**

A scheme of segmentation stage formed by a 2-dimensional array of coupled non-linear oscillators and an inhibitory cell is shown in Figure 6. Each oscillator is associated with one pixel of the previous pre-processing stage.

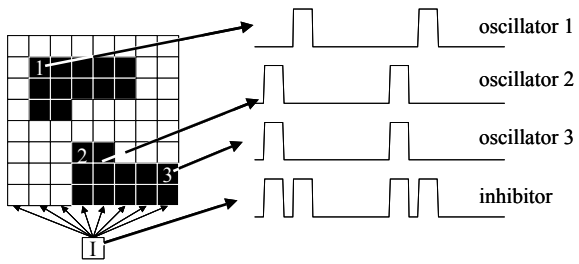



**Figure 6:** LEGION network: Segmentation oscillator array, and drawing of three ideal cells and global inhibitor behaviour.

Object segmentation [5][10] is achieved by two opposed mechanisms: a phase synchronizing effect due to local excitatory coupling of oscillators controlled by adjacent similar pixels and an opposed effect of phase separation due to the global inhibitory oscillator cell.

If two oscillators are associated with two adjacent pixels, an excitatory connection is established depending of luminance similarity. When an oscillator goes active, that is to say, its output voltage is high, it shifts the orbits of adjacent cells that are connected to it and synchronization appears. This is a local mechanism because coupling is only established between adjacent cells and few connections are implemented. By means of these local connections, synchronization is spread to groups of similar luminance and spatially connected pixels, leading to their synchrony.

On the other hand, the global inhibitory cell is responsible of desynchronising pixels. This cell goes active when any oscillator in the network is active. Then, inhibitor shifts orbits of all oscillators in the network so the silent ones –oscillators whose output is low– desynchronise with active oscillators. This mechanism desynchronise groups of oscillators and also prevents random synchronization between them.

In Figure 6, oscillators 2 and 3 become synchronised because there exists an excitatory path among them, by means of the local synapses chain. On the other hand, the global inhibitory cell prevents phase synchronization of separate objects, i.e., oscillator 1 is not in phase with oscillators 2 and 3.

Commonly used oscillators in software implementations [10] are described by two differential equations that can not be easily replicated on a microelectronic design, thus, we have modified these oscillators to be VLSI friendly [5] to occupy less area and consume less power. These oscillators consist of a closed-loop hysteresis comparator and an integrator, as shown in Figure 8.

Implementation of this oscillator is depicted in Figure 7 and it is based in Linares *et al*. [14] current-mode oscillator. Output voltage ($V_{out}$) is the result of integrating currents on the parasitic capacitance of the output node. Transistor M2 drives the threshold current and transistor M1 the input current of the comparator. Hysteresis thresholds are determined by currents $I_{pos}$ and $I_{pos}+I_{wid}$ which are mirrored to transistor M2. The

integrator is made up of a large capacitor ($C_{int}$) that integrates a constant current $I_{dis}$ and a variable current that shifts from 0 to $I_{chr}$ depending on the comparator output. Thus, when it is high, the integrator output voltage increases and when it is low, integrator output voltage decreases. Then, this voltage ($V_{int}$) is converted to a current by transistor M1, that closes the loop.

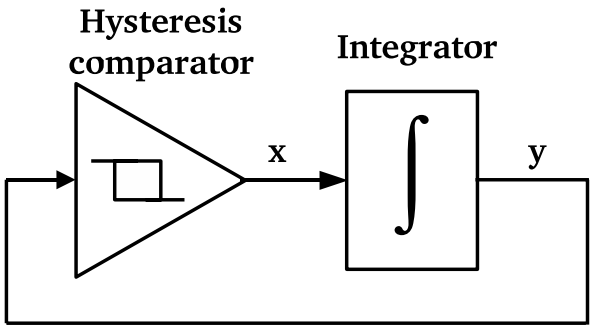



**Figure 8:** Oscillator model.

Coupling can be easily implemented by shifting hysteresis thresholds with transistors M3 and M4a..M4d –one M4 transistor for each adjacent cell–. They charge (M4 transistors) or discharge (M3) when adjacent coupled cells or the global inhibitor are active respectively.

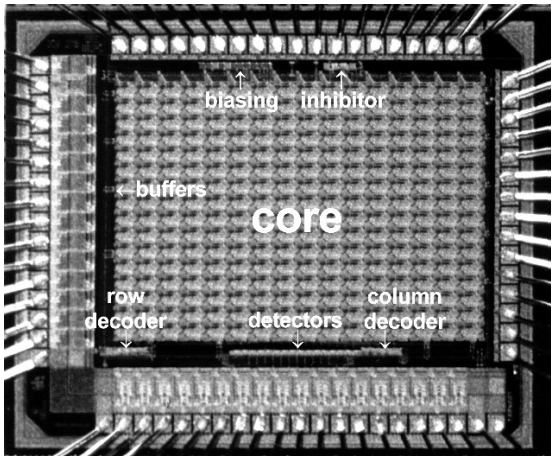



**Figure 9:** 0.8 micron CMOS 16 x16 oscillators segmentation test-chip.

To verify this network functionality, a test-chip containing a 16x16 oscillator array segmentation stage in a 0.8 micron CMOS technology was designed and manufactured (Figure 9) [5]. The chip was fully functional and demonstrated the segmentation ability of the array for binary images. A sample input image and experimental results are shown in Figure 10 and Figure 11. In the latter, single oscillator and global inhibitor waveforms when a four-object input image is used, are shown.

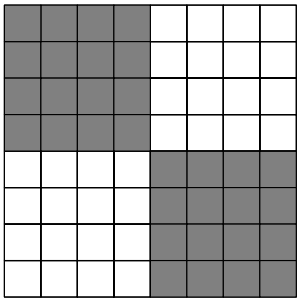


**Figure 10:** Segmentation experimental results – 4-object binary input image.

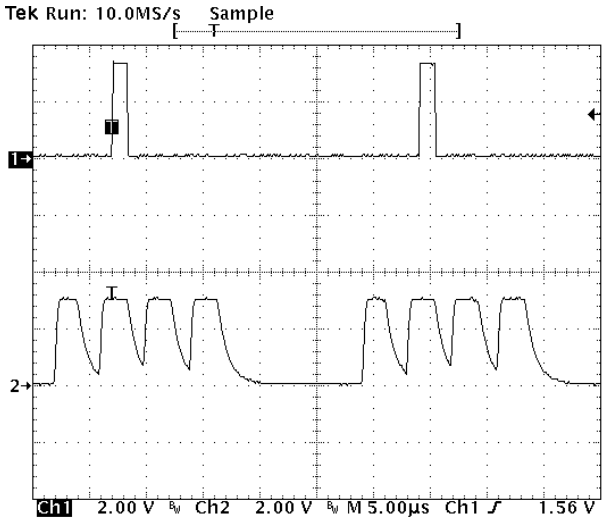



**Figure 11:** Segmentation experimental results – Waveform of an oscillator of the array (upper graph) and global inhibitor (lower graph).

A test-chip layout for the pre-processing and segmentation basic blocks in a more advanced 0.35 micron CMOS technology has also been designed and manufactured to test the oscillator behaviour with this more compact technology (Figure 12). Measurements were performed and results agree satisfactorily with simulations.

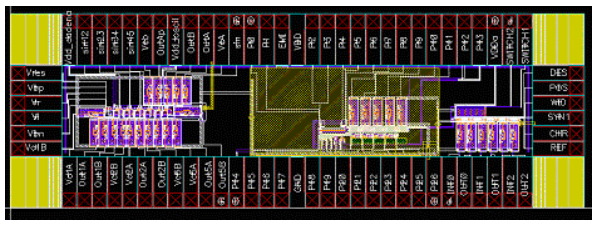


**Figure 12:** 0.35 micron CMOS pre-processing and segmentation basic blocks test-chip layout.

## 5. Output stage

This stage generates results that can be read by a microprocessor or other kinds of processing blocks. The most relevant information that can be obtained from the segmentation system is: image of each segmented object, number of objects and centroid and size of each object.

**a) Segmentation.** The global oscillator high state indicates that all the network oscillators active at that moment belong to the same object. This way, using the global oscillator output as a strobe signal, it is straightforward to obtain the different objects, that are phase-encoded.

**b) Object counting.** Since the global oscillator becomes active (high voltage level) whenever at least a single oscillator of the array is active (high), a simple way to obtain the number of segmented objects in a given image is to count the number of pulses of the global inhibitor during an oscillation period. For instance, in the example of Figure 10 and Figure 11, the number of objects is 4.

**c) Object centroid and size.** When a single object is active, information about its size (number of pixels) and position (centroid) is easily obtained with simple post-processing. Arithmetic addition of currents enabled by active oscillators gives an indication of object size. By means of a resistive diffusion network (stage 7 in Figure 2) the centroid position of each object can be determined.

## 6. Results, conclusions and ongoing work

A complete neuromorphic system for simple vision tasks that require fast and low-power segmentation has been reported. It is based on focal-plane processing using oscillators and analogue circuits. Partial experimental results of the segmentation array and pre-processing basic blocks demonstrate the feasibility of the system. Currently, a functional chip including all the reported stages is in the design process. We expect that in a few months it will be available for experiments. In parallel, a complete system that includes the specific chip and a microprocessor performing digital control of the scene segmentation processor is being specified. This will enable simple applications of vision in portable, low-power applications.

## Acknowledgements

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